Junction Effect on Transport Properties of a Single Si Nanowire Metal–Semiconductor–Metal Device

Sudeshna Samanta, K. Das, and A. K. Raychaudhuri

***Abstract*—We report measurements of electrical transport properties and impedance spectroscopy studies on a single Si nanowire (diameter ~ 50 nm) metal–semiconductor–metal device, fabricated using electron beam deposited Pt. The temperature-dependent four-probe resistivity of the nanowire exhibits freezing of carriers below 30 K, while at higher temperature, it resembles the temperature variation seen in bulk doped crystals. The device shows reproducible nonlinear and asymmetric current–voltage (I–V) characteristics which were quantitatively analyzed and were found to arise from unequal Schottky-type barriers at the two ends which also showed temperature dependence. The measured contact resistance is bias as well as temperature dependent and reduces as the bias is increased.**

***Index Terms*—Electrical transport and impedance spectroscopy, metal–semiconductor–metal (MSM) device, single Si nanowire.**

I. Introduction

THE semiconducting nanoscale structure especially the single nanowire (NW) is interesting to investigate the electrical and optical properties. Exploring the fundamental properties of an individual NW is important as it is a basic unit of any nanoscale device which may arise from size reduction as well as from its large surface to volume ratio. The alignment, manipulation, and connecting a single NW with low-resistive metal electrodes are difficult and challenging too. The dual beam system with metal deposition facility has a very important role in fabricating such single nanodevices. Locating a NW and making contacts on the NW by metal deposition using focused ion beam (FIB) at nanometer level makes such a system a versatile tool for nanolithography. There are several reports [1], [2] on single NW device fabricated by FIB deposited Pt and carbon. The study of such contacts on a semiconducting NW like Si will be very vital since an metal-semiconductor (MS) junction has a large effect in electrical characterization of single NWs. There is a growing interest for the optimization of the contact resistance with low metal electrodes on NWs with ultralow specific contact resistivity [3]–[6]. The contact resistance is appearing due to the presence of the metal electrode and semiconducting NW junction forming Schottky barrier (SB) at each contact. The NW with metal electrodes together form an metal-semiconductor-metal (MSM) device as depicted in Fig. 1. This MSM device contains two back-to-back SBs at the ends where a NW resistance ($R_{\rm NW}$) connects them. The current passing through the MS contact is mainly controlled by the barrier heights and barrier widths of the Schottky contact.

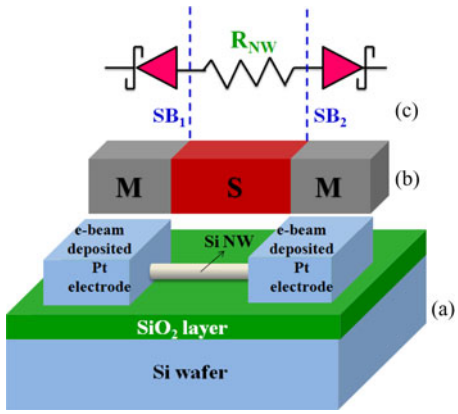

Fig. 1. (a) Schematic diagram of a Si NW with e-beam deposited Pt contact electrodes. (b) Representative MSM structure of the NW device with an equivalent circuit constituted by two Schottky diodes connected back to back with a series resistance $R_{\rm NW}$.

Multiple step photolithography/e-beam lithography patterning and liftoff processes have been used to connect electrodes to an individual single Si NW. The lateral growth-based bridging devices with low contact resistance have also been demonstrated [3], [7]. The quick prototype MSM device can be prepared by FIB deposited Pt. Recently, studies have been reported on temperature-dependent transport properties (current–voltage (I–V) characteristics, contact resistance) on such devices [1], [2]. Till date, however, important issues such as ac transport and impedance spectroscopy have not been addressed to in such single-NW-based MSM devices. In this paper, we address these two new issues. The ac impedance spectroscopy was done to find out the relaxation time of such device and the factors that can limit the relaxation time. In addition to the aforementioned issues, we investigated the temperature-dependent resistivity (ρ) in a four-probe configuration, I–V characteristics, and contact resistance. However, the present investigation is new and it has complementarity to the previous investigation [2] because the Pt electrode used in the present investigation has been grown by an e-beam-assisted deposition of metal from the precursor as opposed to ion-beam-assisted deposition. This is primarily

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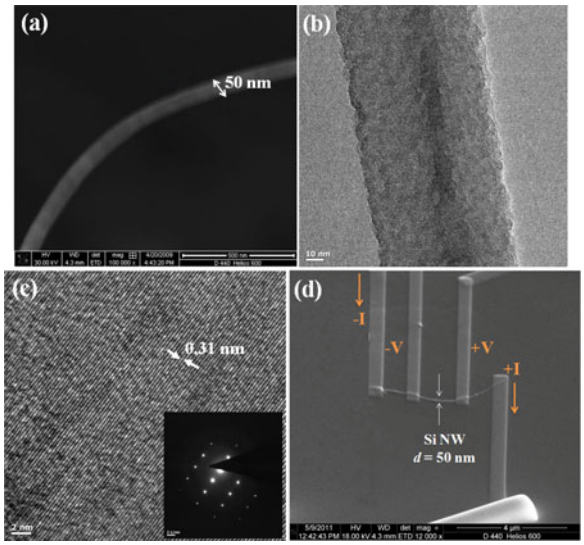

Fig. 2. SEM image of (a) single NW before device fabrication, (b) TEM image of a Si NW, (c) HRTEM image showing lattice fringes. The inset shows SAED pattern, and (d) Single Si NW device with four Pt-electrodes fabricated by e-beam-assisted deposition.

to avoid the Ga ion incorporation and ion-beam-induced amorphization of the Si NW below the contact region.

II. Experimental Details and Results

A. Growth of Si NWs and Device Fabrication

The Si NWs were fabricated by the metal-assisted chemical etching (MACE) technique by immersing p-Si (100) wafers with resistivity of 1 Ω·cm in a solution of 0.03 M $AgNO_3$ and 5.0 M HF in deionized water. The details of the MACE process are given elsewhere [8]. The process leads to formation of a dense array of Si NWs of diameter ranging from $\sim$ 20 to 100 nm and of lengths more than 10 μm. Here, we have used a single NW of diameter $\approx$ 50 nm. The SEM image of a single NW isolated from the ensemble is shown in Fig. 2(a). A transmission microscope (TEM) image is shown in Fig. 2(b). We found the existence of an oxide layer of thickness $\leq$ 2 nm. Fig. 2(c) shows lattice fringes taken with high resolution TEM (HRTEM) and the inset shows selected-area electron diffraction (SAED) pattern. The NWs are single crystalline in nature with lattice constants 0.31 nm that matches with the Si lattice constants for $\langle 1\ 1\ 1 \rangle$ plane.

B. Electrical Measurements

1) Electrical Transport: The temperature (T)-dependent resistivity (ρ–T) data (obtained in a four-probe measurement) of the single Si NW from 10 to 300 K are shown in Fig. 3. The resistivity was measured with a low current of 0.5 μA. The typical ρ of the NW at room temperature is $\approx$0.2–0.3 Ω·cm. The comparison of the ρ with resistivity of bulk Si gives us an estimate of carrier density $n \approx 6\times10^{16}/\text{cm}^3$. For 200 K $\leq T \leq$ 300 K, ρ increases with decrease of T followed by a plateau region for 30 K $\leq T \leq$ 150 K. For $T \leq$ 30 K, ρ increases very sharply with decrease of T indicating onset of carrier freeze out. (The inset of Fig. 3 shows the carrier freeze-out region.) The I–V

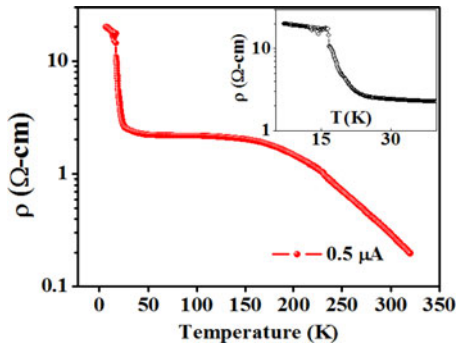

Fig. 3. ρ versus T plot with current bias 0.5 μA. Inset shows that ρ increases sharply below 30 K.

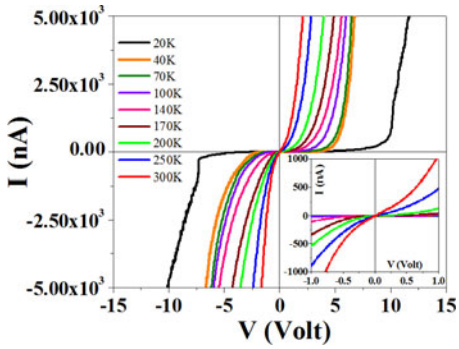

Fig. 4. Nonlinear I–V characteristics of the Si NW MSM device at different temperatures. Inset shows the data at low bias voltages $\simeq \pm$1 V.

measurements were performed on Si NW device by applying dc voltage (V) at different temperatures from 20 to 300 K are shown in Fig. 4. The current in the device (particularly in the low bias region $\leq$ 1 V) reduces sharply to few pA as the temperature is lowered below 70 K. Below the freeze-out temperature, there is a very little measurable device current even at a bias of 10 V. The I–V characteristics are nonlinear and asymmetrical for all the temperatures even at low voltages as shown in the inset of Fig. 4. At the highest device current (10 μA), the current density is $\approx 2.5 \times 10^4$ A/cm^2, which is much less than the electromigration damage threshold. The recorded I–V are reversible and reproducible for a given device on temperature cycling and room storage implying the stability of the Si NW device. The analysis of the data is given in Section III.

The device configuration enables us to do two-probe as well as four-probe measurements at the same temperature in the same device. This allows us to find the contact resistance R_C as a function of bias as well as temperatures. In Fig. 5(a), we show the variation of the specific contact resistance ρ_C ($=A_C R_C$) as a function of T and the bias (A_C is the area of contact). Increase of bias reduces ρ_C substantially. We limited the analysis for bias upto 1 V, because the variation of ρ_C saturates at higher bias. The temperature dependence of ρ_C with T at bias voltage 0.4 V are shown in Fig. 5(b). ρ_C increases on cooling which is a manifestation of the enhancement of the barriers at the contacts as discussed later on.

2) Impedance Spectroscopy: We carried out impedance spectroscopy (using an ac bias of 0.5 V) on the Si NW device.

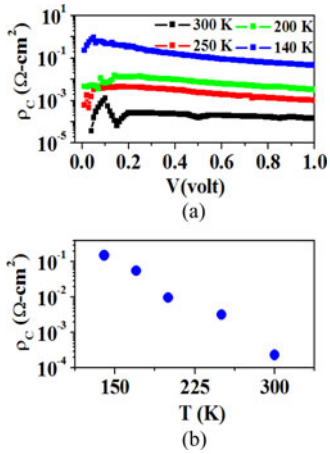

Fig. 5. (a) Bias dependence of specific contact resistance ρ_C at few representative temperatures. (b) Temperature dependence of ρ_C at bias 0.4 V.

The data at the room temperature are shown in Fig. 6. The Data at lower temperatures ($T \leq 280$ K) become dominated by capacitance effects arising mainly from the spurious capacitance from the leads in the device which has SiO_2 dielectric underneath it. Fig. 6(a) shows the impedance Z as a function of frequency (f) from 50 to 10^5 Hz. The frequency dependence of Z is similar to a low-pass filter to a roll off at $f_C \approx 2$ KHz. This can be seen in the Nyquist plot (Z' versus Z'') shown in Fig. 6(b), which shows an almost perfect semicircle. The impedance data have been analyzed using the model shown in Fig. 6(c), where R_1, C_1 are the resistance and capacitance of lead 1 (including the SB at contact SB_1) and R_2, C_2 are corresponding figures for lead 2 (contact at SB_2), respectively. $R_{\rm NW}$ is the Si NW resistance and $C_{\rm sub}$ is the spurious capacitance of the leads arising from the substrate dielectric. The parameters obtained from the model fit are shown in Table I. The dominant contribution that limits the time response arises from the $C_{\rm sub}$, where $f_C \approx 1/2\pi R_{\rm NW} C_{\rm sub}$. A similar kind of parasitic capacitance contribution with same order of magnitude had been reported earlier in impedance spectroscopy experiments on SnO_2 single-NW measurements [9]. The value of the resistivity ρ obtained from direct dc four-probe measurements and that obtained from the model analysis (from R–C network) are plotted together in Fig. 7. The good agreement of the directly measured dc value and that measured from the model, validates the network model for our NW device. It appears that to make the MSM device operate at a higher frequency, the spurious capacitance needs to be reduced substantially.

III. Discussion

The MSM device has two Schottky contacts at the two junctions (SB_1 and SB_2). The I–V data at few representative temperatures have been suitably analyzed as shown in Fig. 8 to find out the barrier heights φ_1 and φ_2 at the two contacts, where φ_1 refers to SB_1 and φ_2 to barrier SB_2 (see Fig. 1). This is under the assumption that the two contact areas are equal. In the MSM device, one junction is forward biased and other is reversed biased. In an ideal condition, (i.e., two equal contact areas, equal

TABLE 1
Electrical Parameters for Si NW Device With MS Junctions From Impedance Spectroscopy at 300 K

R_{NW} (KΩ)	C_{sub} (F)	C_1 (F)	C_2 (F)
800	$(80\pm5)\times10^{-12}$	$(5\pm2)\times10^{-12}$	$(5\pm2)\times10^{-12}$

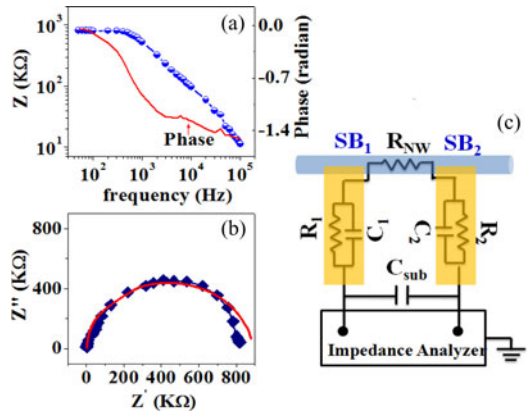

Fig. 6. (a) Plot of total impedance Z and the phase with frequency at 300 K. (b) Nyquist plot Z' versus Z'' for the whole device. (c) Equivalent R–C network for the Si NW device.

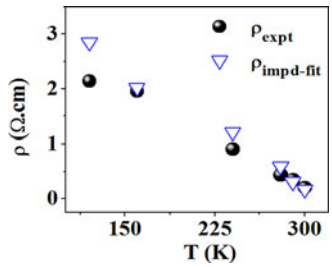

Fig. 7. Comparison of two ρ values obtained from direct dc resistivity measurement and from the R–C model fit of impedance spectroscopy.

amount of Pt deposited at each electrode, and the same adhesion property of electrodes with Si NW) the two Schottky junctions must be identical attributing symmetric I–V characteristics. In our case, the deviation from symmetric nature of the I–V curves arise because of $\varphi_1 \neq \varphi_2$. This inequality arises from the likely differences in the surface conditions at the two ends that will determine the actual value of the barriers. It should be pointed out that the 2-nm-thin SiO_2 layer on Si NW may act as a tunneling barrier which can modulate the transport mechanism with the generation of the leakage current. Here, we excluded the contribution of the tunneling current.

The bias-dependent current I has been fitted with the equation for back-to-back Schottky diodes connected by a resistor [10]

$$I(V) = I_0 \exp\left(\frac{qV'}{\eta kT} - 1\right) \times \frac{\exp(\frac{-q(\varphi_1+\varphi_2)}{kT})}{\exp(\frac{-q\varphi_2}{kT}) + \exp(\frac{-q\varphi_1}{kT})\exp(\frac{qV'}{\eta KT})} \quad (1)$$

where, $V' = V - IR_{\rm NW}$ and I_0 arises from thermoionic emission. The I–V data at low bias (< 0.5 V) as well as the fitted

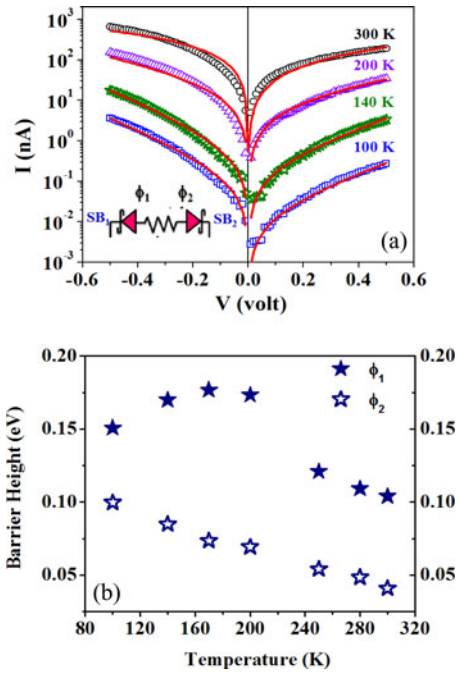

Fig. 8. (a) I–V data with fitted to (1) at few representative temperatures. (b) Variation of barrier heights φ_1 and φ_2 with temperature.

curves are shown in Fig. 8(a). We fitted (1) to the I–V data for obtaining the barrier heights directly from fitting not by the work function of metal and electron affinity of Si [11]. We find that $\varphi_1 \neq \varphi_2$ for all temperatures which will lead to asymmetric I–V curves. We were unable to fit I–V curves for $T \leq 70$ K. The voltage $\pm$ 1 V is not sufficient enough to draw enough current across the device due to high contact resistances at the junctions and the measured current falls below the instrumental resolution. The experimentally obtained barrier heights as shown in Fig. 8(b), we have plotted the variation of the barrier heights as determined from the fit at different temperatures. At the room temperature, $\varphi_1 \approx 0.1$ eV is higher than $\varphi_2 \approx 0.04$ eV. However, φ_1 and φ_2 differ as the device is cooled down. Both φ_1 and φ_2 increase as T is lowered. However, they show saturation at lower temperatures. At lower temperatures, the contact resistances are very high and also the sample is highly resistive. As a result, the values of φ will be prone to error. The enhancement of the barriers at lower temperatures will lead to increased contact resistance on cooling as has been observed [See Fig. 5(b)].

The above analysis of the barrier assumes that in the region of low bias ($\leq$ 0.5 V), the barrier height φ_B of the SB is independent of bias and the only dependence is its T dependence. However, in reality, the barrier can have also a bias dependence. Such an approach has been used in analysis of the barrier in an earlier report [2], where the bias dependence of φ_B has been derived from the temperature dependence of the current measured at different bias. A reverse biased junction current follows the relation [2]

$$I(V) = I_0 \exp\left(\frac{q\varphi_B}{\eta k_B T}\right) \qquad (2)$$

where η is the ideality factor. The value of φ_B obtained by this method is about 25–30% lower than that obtained from the analysis based on (1). The method shows a lowering of the barrier by applied bias. This, however, neglects the dependence of the barrier on temperature. The exact value of the SB thus will depend on the method used for evaluating it. Nevertheless, the values obtained by both methods are within reasonable range, considering that they have been evaluated with very different assumptions and equations.

The ideal SB height at a metal p-type semiconductor junction is given as $\varphi = E_g - (\varphi_m - \chi_s)$ [12], where E_g is the band gap, χ_s is the electron affinity of the semiconductor, and φ_m is the work function of the metal. For the p-type Si used here have $\chi_s =$ 4.05 eV and $E_g \approx 1.1$ eV [12]. For the metal electrode used here, φ_m value will be much less than that of pure Pt (6.4 eV) [11] because of the presence of large amount of amorphous carbon that forms the matrix of the deposited Pt due to the precursor used. Previous studies [13] showed that the volume fraction of carbon can be as large as 70% which estimates $\varphi_m \sim 5$ eV. The estimated ideal barrier then is ~ 0.15 eV, which is close to what we observe.

The barrier height observed in Si NWs will depend on factors like surface charge, image force [2], [14], Fermi level pinning [15], and leakage current by tunneling through thin SiO_2 layer. The surface charges can be immobilized on the surface (SiO_2) shell. Similar to the effect of interface charges on the space charge region of a MS contact, the interface charges at the $Si \setminus SiO_2$ interface in the NW will influence the potential profile and the barrier formation. One of the earlier studies [2] made the contacts using FIB deposited Pt and obtained contacts with ultralow barrier ~ 0.015 eV. This also leads to low specific contact resistance. The image force plays an important role in barrier height lowering and applying the image force theory, we obtained carrier concentration $2\times10^{16}\text{cm}^{-3}$ which matches with the carrier concentration of the Si wafer that we used to prepare our NWs. This confirms the pristine quality of our NWs grown. It has been claimed that the exposure to Ga ions during Pt deposition amorphizes the Si NW in the contact region leading to low barrier formation. In our experiment, the deposition is done by electron beam, thus avoiding ion-beam-induced amorphization and creation of defects. Hence, Fermi level pinning due to disorder can be excluded. The interface states can act as pinning sites there.

The bias and temperature dependence of barrier height would depend on a number of factors primarily on the surface of the Si NW. The formation of the MSM device where the barrier heights can be reproducibly and predictably controlled, would need more control and understanding of surface states on Si NW, which will be a topic of future investigation.

IV. Conclusion

We have fabricated an MSM device based on a single Si NW using e-beam-assisted deposition of Pt electrodes as contacts. We have investigated the temperature-dependent transport properties of the single Si NW device which include four-probe resistivity, I–V characteristics, contact resistance, and ac

impedance spectroscopy. The resistivity shows the behavior of a doped Si with carrier freeze out below 30 K. The nonlinear I–V characteristics were analyzed using a model of two back-to-back Schottky diodes that are formed at the contacts of the Si NW with the deposited Pt electrodes, and hence, we obtained temperature-dependent barrier heights. The difference in barrier heights at the two contacts leads to asymmetry of the measured I–V curves. The device resistance measured at different temperatures and different bias with two-probe and four-probe methods allow us to measure the specific contact resistance ρ_C that evolves with both T and the applied bias. While lowering of T enhances it, applying bias lowers it. The ac impedance measurement showed that the system has a low-pass filter type response with a roll off in the frequency range of few kilohertz that appears to arise mainly from the spurious lead capacitance contributions.

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